FDC-2

A Double Density Floppy Disk Controller for the S-100 Bus

Edition 2

ERRATA
Edition 2, FDC-2 Manual
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The following material will be incorporated into Edition 3 of the FDC-2 Manual.

Disc Drive Power Supplies

Users should be aware that the FDC-2 requires that the disc drive power supply be capable of supporting all system stepper motors simultaneously. A typical requirement for a single drive would be 24 Volts at 1.4 Amps; a four drive system of such typical drives would require 24 Volts at 5.6 Amps. As the manual explains, the drives should be jumpered so that their stepper motors are always enabled and do not require drive select to be enabled.

The advantage of this arrangement is that the FDC-2 can perform simultaneous stepping by rapidly multiplexing drive select from one drive to the next; this rapid multiplexing of drive select, however, is not suitable for the requirements of a stepper motor that is enabled by drive select.

Disk Drive Setup

The user should be aware that user selectable options existing in various manufacturers' floppy disk drives must be correctly selected to insure dependable operation with the FDC2 controller.

Stepper Motor Enable:

For correct operation with the FDC2, the floppy disk drive should be jumpered to have a continously enabled stepper motor. The stepper motor should NOT require active drive select or head load in order to be enabled.
To select this mode of operation in:

Shugart 800/850, Remex 4000, Qume ; open Jumpers HL and DS

Head Load:

For correct operation with the FDC2, the floppy disk drive should be jumpered to load the heads on active head load. The drive should NOT require active drive select to load the heads.
To select this mode of operation in:

Shugart 800/850, Remex 4000, Qume ; close Jumpers C,X,A
open Jumpers B

Multiple Drives:

For correct operation with the FDC2, the floppy disk drive interface signal lines should only have one pullup resistor per line. Usually this involves making sure that the removable pullup resistor pack be removed from all but one drive in a system. However be careful, some drives do not allow this, especially when mixing drives of different manufacturers togethe Often shunt jumpers are provided in the drive to disconnect individual pullu resistors from control lines. When mixing different make drives, it is best to check the manufacturers' documentation.

FDC-2

A Double Density Floppy Disk Controller
for the IEEE 696.2 S-100 Bus

Economical, flexible, efficient mass storage has become a basic requirement for all but the most primitive microcomputer systems. Floppy disks are a recognized standard for this purpose, providing users with not only a means for storage, but for communication as well. The FDC-2 floppy disk controller implements this fundamental mass storage function reliably and elegantly.

Double density, dual head capacity brings large data base processing into the reach of the small system, while direct memory access means that the controller is entirely responsible for data transfer, eliminating the need for wait states and other processing required in less sophisticated floppy disk systems. Conforming to the new IEEE 696.2 S-100 standard, including 24-bit extended addressing DMA, the FDC-2 is entirely upward compatible with the new 16-bit processors, such as Ithaca Intersystems' Series II MPU-8000 Z-8000 CPU card.

The FDC-2 is available with the CP/M™ operating system, for use in standard 8-bit microcomputers. With an Ithaca Intersystems MPU-80 Z-80 card and IEEE S-100 extended addressing memory, 8080/Z80 application programs can use a megabyte of address space, all of which can be directly loaded by the FDC-2 floppy disk controller (under application program control).

Adaptable to 5-1/4" and 8" drives, compatible with old and new S-100 systems, the FDC-2 provides the microcomputer designer and user with a mass storage interface for most current and anticipated floppy disk applications.

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1.0 Introduction and General Information

The Intersystems Floppy Disk Controller (FDC-2) is a powerful and versatile mass storage system for the S-100 computer. The FDC-2 offers the following features:

* Up to 4 Mbyte direct access mass storage
* Single or Double Density
* Soft Sector IBM compatible
* 8" or 5.25" disks, single or double sided
* 1 thru 4 drives controlled by one board
* LSI controller with extensive instruction set including disk to memory compare instructions
* DMA data transfers between disk and system memory relieve CPU of cumbersome transfer routines
* Efficient operation allows entire track contents transferred in one disk revolution
* On board EPROM
* CPM compatible
* IEEE 696.2 S-100 compatible including:
  2 or 4 MHz operation;
  8 or 16 bit I/O mapping;
  16 or 24 bit memory mapping for EPROM;
  16 or 24 bit DMA.

1.1 Service Information

Receiving Inspection

When your FDC-2 arrives, inspect both the equipment and the shipping carton immediately for evidence of damage during transit. If the shipping carton is damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened, and the contents of the carton are damaged, save the carton and packing material for the agent's inspection. Shipping damages should be immediately reported to the carrier. Do not attempt to service the board yourself as this will void the warranty.

We advise that in any case you should save the shipping container for use in returning the module to Intersystems, should it become necessary to do so.

Factory Service

Intersystems provides a factory repair service for all of its products. Before returning the module to Intersystems, first obtain a Return Authorization Number from our sales department. This may be done by calling us, sending us a TWX, or by writing to us. After the return has been authorized, proceed as follows:

1) Write a letter describing the problem as best you can.

2) Describe your system to us, list boards by manufacturer and name.

3) Include Xerox copies of the schematics of boards by manufacturers other than Intersystems.

4) Include the Return Authorization Number.

5) Pack the above information in a container suitable to the method of shipment.

6) Ship prepaid to Intersystems.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

Contacting Intersystems:

The following apply both for correspondence and service.

Ithaca Intersystems Inc.
1650 Hanshaw Rd.
P.O. Box 91
Ithaca N.Y. U.S.A.
14850

Telephone (607) 257-0190
TWX 510 255-4346

In Europe:

Ithaca Intersystems (U.K.) Ltd.
58 Crouch Hall Rd.
London N8 8HG. U.K.

Telephone 01-341-2447
Telex 299568

1.2 Overview

The FDC-2 may be instructed, through a series of output operations, to perform two basic functions: read data from anywhere in memory and write it at a desired drive, side, sector, and track; and the inverse function of reading specified disk data and writing it at any desired location in system memory.

The FDC-2 provides a modern disk interface for the S-100 bus. A single 8", double density, single sided disk provides the user with approximately 500 kbytes of mass storage. Since the controller board is capable of handling 4 double sided disks, 4 Mbytes of mass storage is available.

The FDC-2 may be parsed out into separate functional areas for easier understanding. These are:

Disk Controller

This area of the FDC-2 interfaces directly with the disk drives. It can be instructed by the CPU to select one of four drives, move the recording head in a specified drive to a specified track position, read a specified quantity of data from a drive, write a quantity of data to a drive, format a disk, and even compare data on the disk to system data. The controller also performs CRC checks on all disk data to establish that data's validity.

DMA Controller

This functional area of the FDC-2 is dedicated to the direct transfer of data between the Disk Controller and the user's system memory. The DMA controller has the ability to disable the system CPU asynchronously to program execution, whenever the Disk Controller indicates readiness for data transfer. Once the CPU is disabled the DMA Controller will either read a byte from system memory and send it to the Disk controller, or read a byte from the Disk Controller and write it into system memory. After the DMA transfer, the CPU is re-enabled and will continue program execution. The user may program the DMA Controller to access any area of an IEEE 696.2 S-100 16 Mbyte address space.

Addressing

The FDC-2 occupies 16 consecutive locations of system I/O space. The function assignment of each of these locations is shown in the FDC-2 Address Map. The user may jumper select the board location at any 16-location boundary in the standard IEEE S-100 64k I/O space. Optionally, of course, the 8-bit I/O address space may be referenced instead.

Onboard EPROM

Provision is made for a 2708 EPROM on the FDC-2 so that bootstrap firmware for the user's operating system may be located on the board. The EPROM circuitry has its own independent address. The user may jumper-select any 1 kbyte location in the extended 16 Mbyte system memory to locate the EPROM. The board may be configured so that PHANTOM is driven when the EPROM is accessed, thus allowing the FDC-2 EPROM to overlay RAM memory that responds to PHANTOM; the EPROM -- and the PHANTOM overlaying signal -- may be disabled with software. (The EPROM is enabled automatically when power is applied and RESET* goes active.)

1.3 FDC-2 Address Map

Base address is set to 00H.

Address (hex)		Function	
Base:	00	Disk Controller Status/Command	(R/W)
	01	Disk Controller Data	(R/W)
	02, 03	set DMA write to system memory*	(W)
	04, 05	set DMA read from system memory*	(W)
	06, 07	enable EPROM*	(W)
	08, 09	DMA upper address byte*	(W)
	0A, 0B	DMA middle address byte*	(W)
	0C, 0D	DMA lower address byte*	(W)
	0E, 0F	disable EPROM*	(W)

* In each of these cases, either port listed will perform the specified function and may be used interchangeably; that is, the FDC-2 disregards A0.

1.4 Floppy Disks and Floppy Disk Operating Systems

A floppy disk is a round piece of plastic mylar coated with a magnetic recording film -- much like the material magnetic recording tape is made out of, only stiffer and shaped like a phonograph record. A floppy disk, in fact, has some of the advantages of a phonograph record: access to any part of the disk is relatively quick, much like picking up the needle of a phonograph record and moving it to another band. This is inherently faster than reel-to-reel tape or cassettes, where it is necessary to run through the reel to get to a particular piece of data.

The plastic disk is permanently encased in a square paper or cardboard jacket. It is never removed from this jacket. The disk may be inserted into a disk drive which rotates the disk inside the jacket. The drive also contains a high quality playback/recording head which can be loaded into contact with the disk. The head is affixed to some sort of mechanism that allows it to move along the radius of the disk. The force for this movement is usually provided by a stepper motor, so that the head is moved incrementally from one "track" to another. On an 8" disk, there are 76 of these tracks available for data storage. On such a disk, roughly 6.5 kbytes can be stored serially on a single "track" when recorded in double density. Usually, this data is organized in smaller "sectors": angular portions of the whole track. Various systems use various numbers of sectors; a standard CP/M™ single density disk has 26 sectors.

Operating Systems

The term "operating system" (OS) refers, broadly, to any software that allows a human being to interface with a computer system. A floppy disk operating system obviously implies interface to a disk device as well as the computer.

The operating system is the thing that prints the asterisk, period, or other prompt character on the terminal when the user first turns the computer on. This is one of the customary tasks of an OS: it is the first major program to get control. (Most disk operating systems actually have one or more "bootstrap" programs that initially load the operating system into memory before passing control to it.)

The EPROM monitors that some computer companies market are, in fact, simple operating systems. A simple program of this kind allows the user to communicate with the computer at a relatively primitive level, usually providing load and dump memory instructions so that programs may be loaded directly in machine language. The monitor provides a basic communication facility by containing software that handles a terminal -- where the user types his instructions to the monitor and reads the data the monitor gets.

A disk operating system is an elaborate monitor. It also provides the basic function of terminal communication with the user. In addition, of course, it provides facilities for getting and loading data to and from disks. Other features are provided by various operating systems, from assembler software (a program that will translate a file filled with symbolic assembly code written by the user into machine code suitable for execution) to facilities for multi-tasking, various high-level languages, and so forth.

Operating systems are commonly designed to be modular: that is, programs can be added later on, either by the user or by the manufacturer. The operating system will often be provided with a few modular parts already included, usually the most-needed basic programs, and these programs are referred to as "utility programs" or just "utilities". A program that prints a specified disk file on the system line printer, for instance, would be a utility. Various operating systems assign different functions to the OS directly, leaving other functions to the utilities. One OS, for instance, might provide the listing function as an OS instruction; another would require that a utility program be loaded first to execute the same kind of function.

One extremely popular operating system is the CP/M™ system. The advantages of using CP/M™ can really be summed up in one word: compatibility. Programs that operate in a CP/M™ environment are available from many different sources, and users of CP/M™ can exchange data and user-written programs with ease, merely by trading disks.

Although all standard CP/M™ disk files are compatible, all CP/M operating systems are by no means identical. Each CP/M™ system has certain individual characteristics. One of these is memory size: a program designed to run on a large CP/M™ system will not execute successfully on a small one, because there is simply not enough memory. The other significant variable is the input/output (I/O). The CP/M™ manual gives more details on this topic, but suffice it to say that every different piece of I/O hardware requires a corresponding adjustment in the operating system; one manufacturer's disk controller will require different software than another's, and the same is true of different terminal interfaces (although the modification of the terminal handling part of the code is usually much easier than changing the disk handling portion). Ithaca Intersystems, of course, offers a version of CP/M™ that runs with the FDC-2 Disk Controller Board.

Section 2

Board Setup

2.1 I/O Addressing

2.2 EPROM Addressing

2.3 Wait States

2.4 Interrupts

2.5 DMA

2.6 Standard or Mini Disk Drive

2.7 Precompensation

2.8 Notes on Drive Configuration
- Stepper Motor Enable
- Head Load
- Multiple Drives

2.9 Standard Ithaca Intersystems Board Setup

2.0 Board Setup

The user should select and check the various jumper selectable options on the FDC-2 board before inserting the board into the user's S-100 system. The jumper selectable options include:

* I/O Addressing
* EPROM Addressing
* Wait State Selection
* System Interrupt Line Selection
* DMA Configuration
* 8" or 5.25" Disk Drives
* Precompensation Values

2.1 I/O Addressing

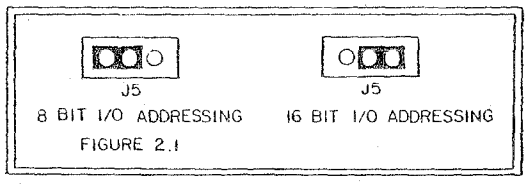


FIGURE 2.1

The user should select the board I/O address to correspond with the system hardware and software. First, the user should set the board for either 8 bit or 16 bit I/O addressing. This decision should be based upon what I/O addressing the system CPU uses. Shunt jumper J5 selects between 8 or 16 bit I/O addressing. See Figure 2.1.

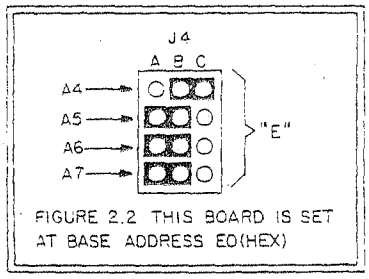


FIGURE 2.2 THIS BOARD IS SET AT BASE ADDRESS E0(HEX)

Secondly, the user should select the board I/O address. If the board is 8 bit addressed, then only jumper area J4 affects board address. The user may select address bits 4 through 7. See Figure 2.2.

Finally, if the board is 16 bit I/O addressed, then jumper area J19 affects the upper 8 bits of board address, A8 through A15. See Figure 2.3.

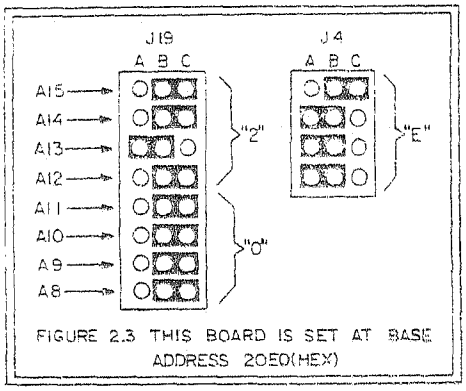


FIGURE 2.3 THIS BOARD IS SET AT BASE ADDRESS 20E0(HEX)

2.2 EPROM Addressing

The user must set the EPROM memory address to correspond to system hardware and software. Jumper area J20 determines the enabling and the base address. The options are:

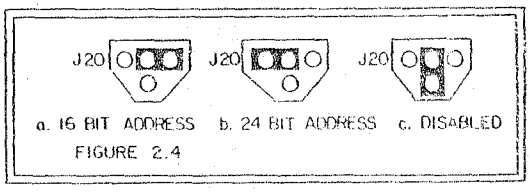


FIGURE 2.4

* The EPROM is enabled and has a 16 bit base address.
* The EPROM is enabled and has a 24 bit base address.
* The EPROM is disabled.

See Figure 2.4.

The EPROM address itself is selected at jumper area J21. For 16 bit addressing, J21 is used to set address bits 10 to 15. See Figure 2.5.

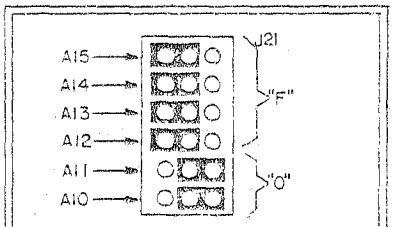


FIGURE 2.5 THIS BOARD'S EPROM IS LOCATED AT F000(HEX)

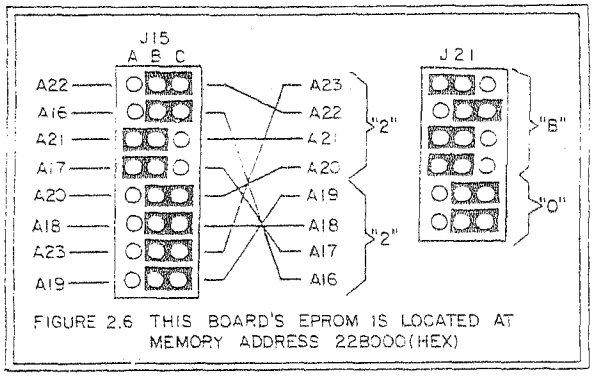
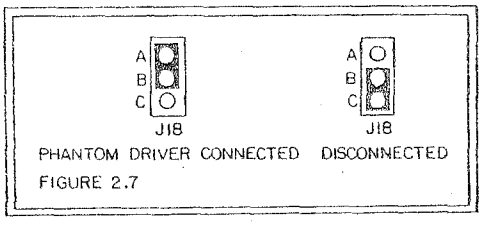


FIGURE 2.6 THIS BOARD'S EPROM IS LOCATED AT MEMORY ADDRESS 228000(HEX)

If 24-bit addressing is being used in the system, then J15 must also be set to correspond to address bits A16 through A23. See Figure 2.6.



PHANTOM DRIVER CONNECTED DISCONNECTED
FIGURE 2.7

Finally, the user may decide if the EPROM will be phantom memory or not. If the EPROM is phantom, it will drive the S-100 phantom line when it is selected, disabling any other memory that may happen to be located at the same address, avoiding conflicts on the bus that might occur between the EPROM and read/write memory. Note that the FDC-2 EPROM may be disabled by software after power on (the reset which occurs at power on automatically enables the EPROM): writing to a port on the board provided for this purpose disables the EPROM, while writing to an additional port provided will subsequently enable it, if desired (see the FDC-2 address map in section 1). This allows the EPROM to be used for a bootstrap load of the operating system after which it may be turned off, freeing that space for RAM. To enable the phantom driver, use J18 as shown in Figure 2.7.

2.3 Wait States

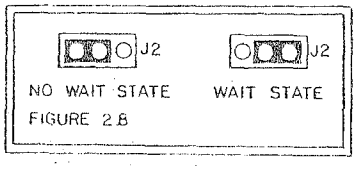


FIGURE 2.8

When running in a 4 MHz system the EPROM and the LSI disk controller may not have sufficient access time for valid data transfers with the CPU. If this is the case the user should set jumper area J2 so that the FDC-2 generates one wait state at each access. See Figure 2.8.

If the board is set to generate a wait state at access, then the polarity of the system clock Phi becomes significant. Jumper area J14 provides for either the IEEE 696.2 S-100 standard clock, or a non-standard inverted clock. See Figure 2.9.

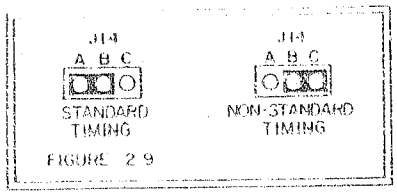


FIGURE 2.9

2.4 Interrupts

The FDC-2 generates an interrupt signal at the end of various procedures so that the system CPU can respond to the event with appropriate action. The S-100 bus provides 10 interrupt lines: NMI, pINT, and the vectored interrupt lines VI0 through VI7. The FDC-2 interrupt signal may be jumpered to any one of these, with the exception of NMI (which is customarily reserved for emergency system functions such as power failure processing).

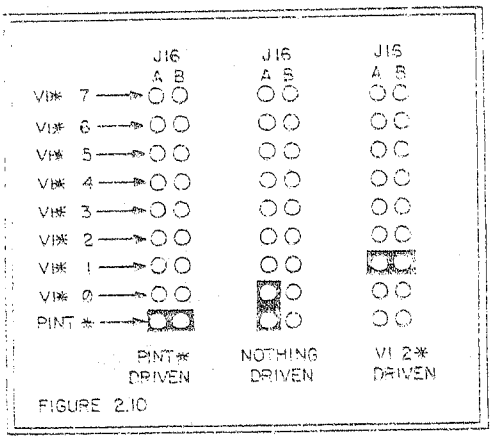


FIGURE 2.10

If there is a system interrupt controller (on the CPU card, perhaps) the FDC-2 and other system peripherals might drive one or another of the vectored interrupt lines. Alternately, in a system without an interrupt controller the FDC-2 can be jumpered to drive pINT. In either case, of course, software must be available to deal with interrupts. In the case of vectored interrupts, generally the interrupt controller device is initialized, and interrupt service routine address vectors stored there. In the case of a pINT system, care must be taken that no other device in the system drives the pINT line, and that no device in the system responds to the interrupt acknolwedge signal, sINTA. If these conditions are met, then the FDC-2's interrupt will cause the CPU to read and execute a byte of FFH, which, in 8080 code, is a RST 38H. Alternately, a Z80 processor may be set to Interrupt Mode 1, in which case interrupts automatically generate a RST 38H, regardless of the response byte. Location 38H would then contain the interrupt service routine or a jump to one. In a minimal system, the CPU could enter a halt state after it initiates a disk operation; in this case, the interrupt routine at 38H could simply be a RET instruction.

An entirely different -- and in many cases, simpler -- approach to software response to disk board activities is the use of the Polled Mode. In this case, the FDC-2 drives no interrupt line at all, and the CPU executes a short polling routine while floppy disk operations are carried on.

Jumper area J16 is provided to select which system interrupt line -- if any -- will be driven by the FDC-2. See Figure 2.10. In the event that no interrupt line is to be driven, the shorting strip may be stored on any two pins in column A of J16.

2.5 DMA

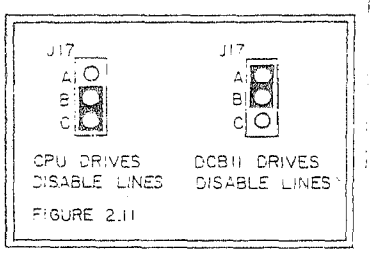


FIGURE 2.11

In some systems, the DMA disable lines -- ADSB, DODSB, SDSB, and CDSB -- will be driven by the CPU card. Other systems expect the DMA device to drive these lines. The FDC-2 makes provision for both possibilities at jumper area J17. See Figure 2.11.

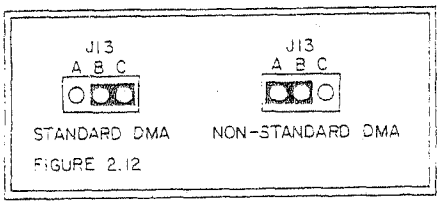


FIGURE 2.12

The IEEE 696.2 S-100 standard provides for overlapped transfer at either end of a DMA operation. Pre-standard CPUs may instead conduct an immediate transfer. To adapt to these differences the FDC-2 may be jumpered at J13 to either turn off the hold signal at the standard point of the DMA cycle, or to extend the hold signal one half clock cycle, to conform to non-standard CPUs. See Figure 2.12.

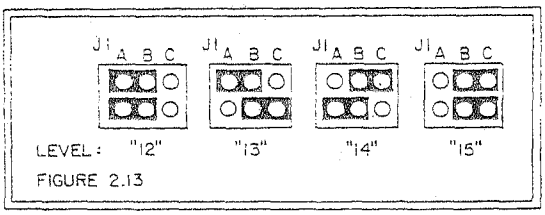


FIGURE 2.13

The standard also provides for 16-level arbitration among DMA devices. The FDC-2 provides the user with the option to occupy any one of the top four DMA priority levels -- levels 12 through 15. The priority level may be selected at jumper area J1, as depicted in Figure 2.13.

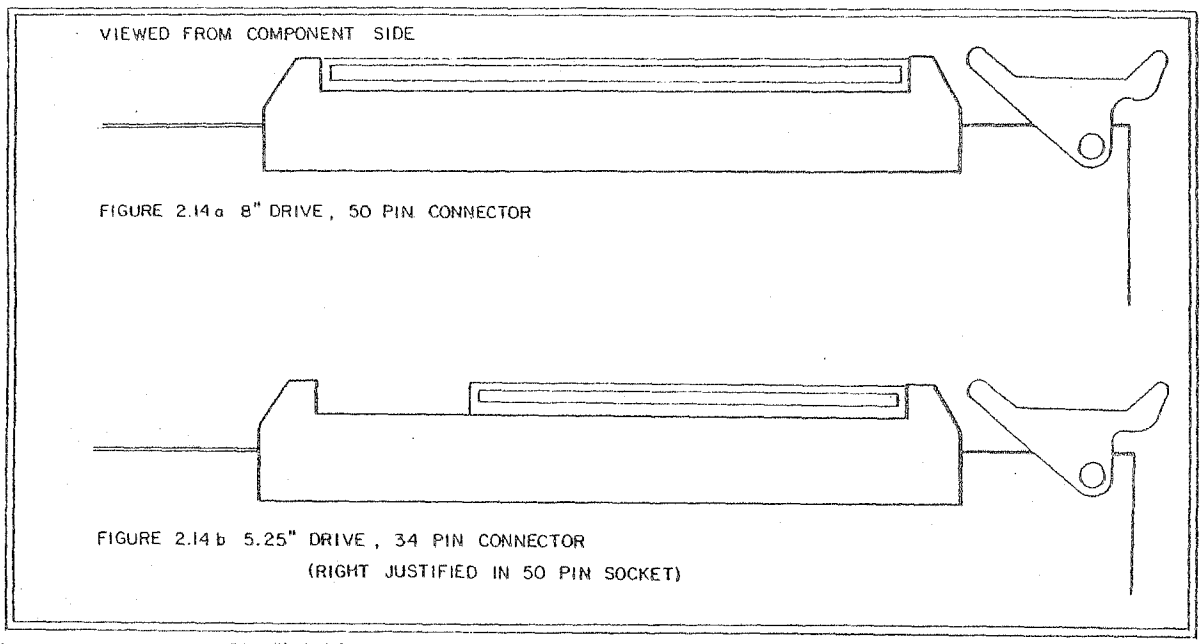


FIGURE 2.14a 8" DRIVE, 50 PIN CONNECTOR

FIGURE 2.14b 5.25" DRIVE, 34 PIN CONNECTOR
(RIGHT JUSTIFIED IN 50 PIN SOCKET)

2.6 Standard or Mini Disk Drive

The FDC-2 can control 8" disk drives or 5.25" disk drives. The 50-pin header on the top right of the board will accept the standard 50-pin connector for the 8" drive or the standard 34-pin connector right justified in the header for the 5-1/4" drive. See Figure 2.14

Various signals must be adjusted to correspond to 8" or 5-1/4" drives. These should be set by the user at jumper areas J6 through J12 as shown in Figure 2.15.

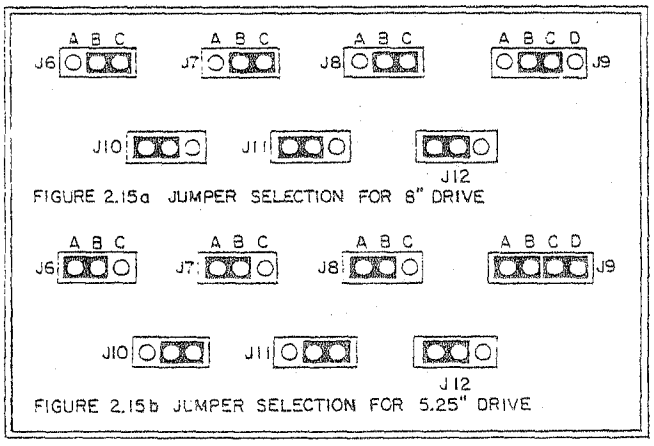


FIGURE 2.15a JUMPER SELECTION FOR 8" DRIVE

FIGURE 2.15b JUMPER SELECTION FOR 5.25" DRIVE

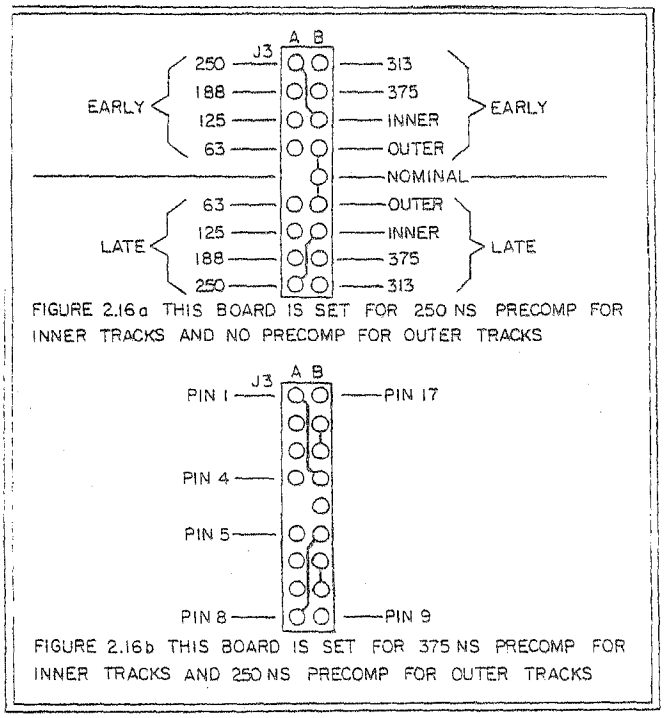


FIGURE 2.16a THIS BOARD IS SET FOR 250 NS PRECOMP FOR INNER TRACKS AND NO PRECOMP FOR OUTER TRACKS

FIGURE 2.16b THIS BOARD IS SET FOR 375 NS PRECOMP FOR INNER TRACKS AND 250 NS PRECOMP FOR OUTER TRACKS

2.7 Precompensation

Precompensation is a slight shift that is imposed on the position of data pulses as they are written on the disk. This is done to compensate for expected shift when data is read back, due to the resolution of the drive head.

Drive manufacturers provide precompensation values to be used with their drives for double density data. The FDC-2 may be jumpered for six different values from 62 to 375 ns. The user may also set one value for inside tracks, and a different value for outside tracks. This can provide additional reliability with many drives. Figure 2.16, a and b, shows various precompensation options at jumper area J3.

2.8 Notes on Drive Configuration

User-selectable options of various manufacturers' floppy disk drives must be set correctly to insure dependable operation with the FDC-2 controller.

Stepper Motor Enable

For correct operation with the FDC-2, the floppy disk drive should be jumpered to have a continuously enabled stepper motor. The stepper motor should NOT require active drive select, and/or head load, in order to be enabled.

Stepper Motor Enable	
Shugart 800/850, Remex 4000, Qume	Jumper HL: Open DS: Open

Head Load

The floppy disk drive should be jumpered to load the heads on active head load alone. The drive should NOT require active drive select to load the heads.

Head Load	
Shugart 800/850, Remex 4000, Qume	Jumper C: Closed X: Closed A: Closed B: Open

Multiple Drives

The FDC-2 (and most other disk controllers) require that the floppy disk drive interface signal lines should only have one pullup resistor per line. Usually this involves removing the pullup resistor pack from all but one drive in a system. This is not always true, however, and problems will sometimes arise, especially when mixing drives of different manufacturers in one system. Often shunt jumpers are provided in the drive to disconnect individual pullup resistors from control lines. Check the manufacturer's documentation carefully, particularly when mixing different manufacturers' drives. Improper termination -- when more than one resistor is pulling up a line, or if no resistor is pulling up a line -- will sometimes result in intermittent operation of the system, ranging from very occasional errors to continuously "flaky" response.

When there is a choice, it is usually good practice to terminate the drive in a multiple-drive system that is furthest -- physically, along the common connector cable -- from the FDC-2; that is, the last drive on the cable, whether it is drive A or not. This last drive, then, would be the one in which an optional resistor pack should be left installed, or the jumpers set so as to enable the pullup resistors.

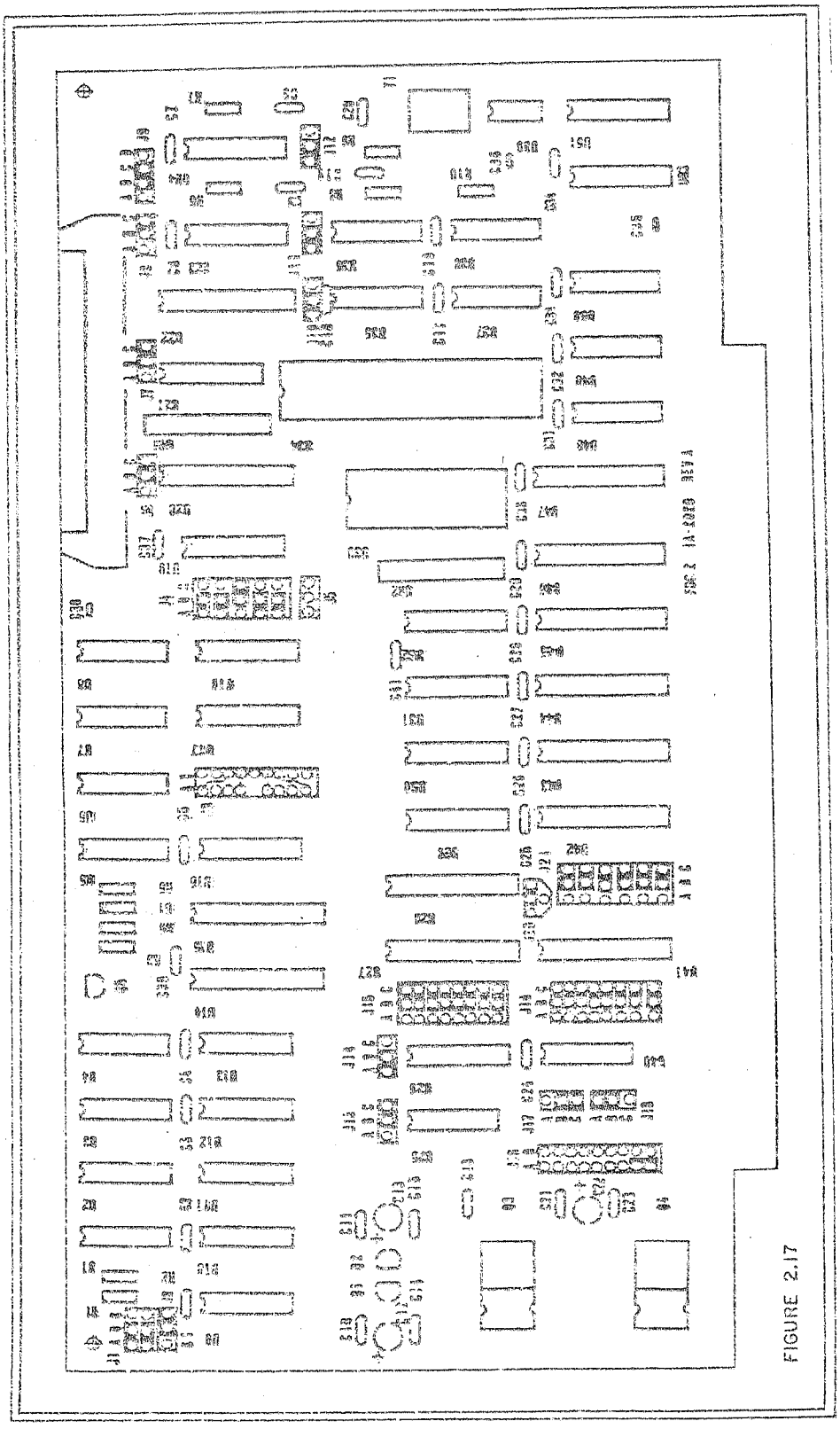


FIGURE 2.17

MANJG3.TXT version 3/05D
edited 4/14/80 3:28 p.m.--jgo edited 4/30/80 12:19 p.m. -- jgo
Second Edition
edited 6/03/80 12:12 a.m. -- jgo
Figure 2.9, 2.15a, 4.1 are changed;
DMA error revisions and applicability
Finney's cxs
parts changes
This symbol -- ™ -- will be a TM when it grows up.

2.8 Standard Ithaca Intersystems Board Setup.

Figure 2.17 shows the arrangement of jumpers for the standard Ithaca Intersystems setup, as listed below.

Implemented Option	Jumper
DMA Priority 12	J1, 1st row: AB 2nd row: AB
One wait state	J2: BC
MFM Precompensation -- inner tracks: 256 ns outer tracks: 62.5 ns	J3: pins 1 to 15, pins 4 to 14, pins 5 to 12, pins 8 to 11
Board address = B0H	J4, 1st row: AB 2nd row: AB 3rd row: BC 4th row: AB
8 bit I/O Address (no extended address)	J5: AB
Standard 8" drive	J6: BC
	J7: BC
	J8: BC
	J9: BC
	J10: AB
	J11: AB
	J12: AB
Standard DMA timing	J13: BC
Wait states clocked on inverted Phi	J14: AB
EPROM extended address = 00H	J15, all rows: BC
No interrupt lines driven	J16, jumper stored on any two pins of row A
No bus disable lines driven	J17: row 2-row 3
EPROM select drives PHANTOM	J18: row 1-row 2
I/O extended address = 00H	J19, all rows: BC
EPROM enabled, 16 bit address (no extended address)	J20, 1st row: BC
EPROM address = 0000H	J21, all rows: BC

Section 3

FDC-2 Programming Guidelines

3.1 Programming the NEC uPD765

3.2 Polled Operation

3.3 Programming DMA Transfers

3.4 EPROM Programming

3.0 FDC-2 programming guidelines

In most cases the user will obtain a FDC-2 board with the operating system software at the same time, and will not be concerned with the details of the implementation. This section is for those who wish to write their own software to drive the FDC-2.

Three areas of the FDC-2 are affected by programming. These are the LSI controller chip itself, the DMA transfer circuitry, and the EPROM. Refer to the FDC-2 I/O map for address location of onboard registers.

3.1 Programming the NEC uPD765

The major part of the FDC-2 operation is conducted by the NEC uPD765, an LSI double density disk controller IC. The uPD765 has a repertoire of 15 different operations which the CPU may instruct it to perform. These are:

Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format Track	Sense Drive Status

The details of this intruction set are explained in the NEC uPD765 manual, to which the interested reader is referred. A quick summary is presented here to relate the uPD765 operation to the rest of the FDC-2.

As the uPD765 performs an operation, there are three phases which must be considered by the programmer. These are:

Command phase: This phase exists for all operations. In this phase the CPU sends command bytes to the uPD765 to indicate which operation is desired and the arguments of the operation (drive, track, sector, etc.). The uPD765 requires that the CPU check the main status register for an active request for master (bit 7 high) and a data input condition (bit 6 low) before each command byte is sent. When the uPD765 recognizes a complete command byte string it will automatically enter the execution phase.

Execution phase: After the uPD765 accepts the command string it will begin to perform the operation. No software interaction is necessary during this phase. If the operation encompasses data transfer between the system and the disk (during read, write, scan, or format), the DMA hardware on the FDC-2 board

conducts the transfer with system memory, and should be programmed prior to the execution phase (programming DMA is covered below). The uPD765 will generate an interrupt signal at the end of the execution phase on operations where data transfers take place as well as seek and recalibrate operations. This interrupt may be serviced by the system in any fashion suitable to the user's requirments.

Result phase: After the execution phase, most operations of the uPD765 enter the result phase. At this point, the uPD765 provides the user with status concerning the success of the operation just attemped: a string of bytes is (and must be) transferred between the uPD765 and the system CPU. These bytes are the status bytes which are described in the uPD765 manual. The CPU must check the main status register for an active master request (bit 7 high) and data in to the CPU (bit 6 high) before reading each status byte in the result phase. The uPD765 will not accept new commands until the correct number of status bytes are read to complete the result phase of the last operation.

3.2 Polled Operation

While the uPD765 is frequently used in the interrupt mode (the chip produces an interrupt to signal the completion of an activity), polled operation is also possible, and in some configurations is desirable. The uPD765 can be polled by checking various chip registers repeatedly. The following code is typical.

```
1000*1000                ORG     1000H

     00B0        DBASE   EQU     0B0H
     00B0        DSTAT   EQU     DBASE+0
     00B1        DDATA   EQU     DBASE+1
     00B2        DREAD   EQU     DBASE+2
     00B4        DWRITE  EQU     DBASE+4

                 ;THIS ROUTINE WOULD BE CALLED AFTER A DISK
                 ;READ OR WRITE HAD BEEN INITIATED.
```

```
1000 DB B0        WAITFDC IN      DSTAT   ;A GETS THE DISK STATUS.
1002 CB 67                BIT     4,A     ;TEST BIT 4 FOR ZERO.
1004 CA 100F              JZ      ERROR   ;IF BIT 4 IS NOT HIGH, THEN
                            ;THE UPD765 IS NOT EXECUTING A READ OR
                            ;WRITE AND THIS ROUTINE WAS CALLED IN ERROR.
1007 E6 C0                ANI     0C0H    ;DISCARD ALL BUT BITS 6 AND 7.
1009 FE C0                CPI     0C0H    ;TEST THEM.
100B C2 1000              JNZ     WAITFDC ;IF BOTH ARE NOT HIGH, WAIT.
                    ;BIT 6 INDICATES THE DATA TRANSFER DIRECTION THE
                    ;NEC 765 IS CONTEMPLATING, AND BIT 7 IS HIGH WHEN THE
                    ;DISK CONTROLLER CHIP IS READY FOR DATA TRANSFER.
                    ;BOTH THESE BITS WOULD BE HIGH WHEN THE NEC765 HAD
                    ;COMPLETED A READ OR WRITE OPERATION AND WAS
                    ;READY FOR THE RESULT PHASE.  "DATA TRANSFER"
                    ;HERE REFERS TO THE PROCESS OF READING OR WRITING
                    ;STATUS OR COMMANDS TO THE NEC765'S DATA
                    ;REGISTER, NOT TO BE CONFUSED WITH THE ACTUAL
                    ;TRANSFERS OF DATA FROM OR TO THE FLOPPY DISK,
                    ;WHICH HAS PRESUMABLY BEEN ACCOMPLISHED BY DMA
                    ;OPERATIONS WHILE THE WAIT LOOP HAS BEEN FUNCTIONING.
100E C9                   RET             ;OVER.
```

To poll the uPD765 while it is executing a SEEK operation, the program would continually execute a sense interrupt status command, and then check the DSTAT register for the four busy signals (by ANDing the byte with 0FH); the seek is complete when the uPD765 is no longer busy.

3.3 Programming DMA Transfers

The DMA control circuitry automatically responds to any DMA request from the uPD765 by activating the S-100 hold signal. When acknowledged by the CPU the DMA circuit will generate one S-100 memory access cycle. It is up to the user's program to establish the address to be accessed and the direction of the transfer.

There are three DMA address registers on the FDC-2, providing for 24-bit extended addresses. When written to by the user's program these registers form a DMA address pointer. The next FDC-2 DMA cycle will access this address. After a DMA cycle this pointer will be automatically incremented to point to the next memory address. The DMA circuitry will access consecutive addresses in memory until the user program again writes to the FDC-2's address registers. The FDC-2 DMA address pointer only increments the 16 least significant bits; consequently, DMA transfers are limited to 64k boundaries in system memory. The upper 8 bits of the 24 bit DMA address pointer must be incremented in software.

A DMA cycle may be one of two types -- a read or a write. In the former case, the FDC-2 reads data from system memory and sends this data to the uPD765 (usually for writing on the disk). In a DMA write, the FDC-2 gets data from the uPD765 (which is reading from the disk) and sends this data to memory. The user's program selects the type of DMA cycle. To select a read-from-memory / write-to-disk DMA cycle, the software need only execute an output instruction to the "set DMA memory read" port. To select a read-from-disk / write-to-memory cycle, the software need only execute an output instruction to the "set DMA memory write" port.

3.4 EPROM Programming

EPROM programming consists of enabling and disabling the EPROM. If the FDC-2 is shunt selected with the onboard EPROM enabled, then the EPROM will be enabled after system reset. The user's software can disable the EPROM by simply executing an output to the FDC-2 "disable EPROM" port. The software may re-enable the EPROM by simply executing an output instruction to the FDC-2 "enable EPROM" port.

Section 4

Parts List and Placement

4.0 Parts List and Placement

Figure 4.1 shows the placement of parts on the FDC-2, as specified in the following charts.

RESISTORS

Position	Value	Tolerance	Power
R1, R2	1 KOhm	10%	1/4 W
R3	2.4 KOhm	10%	1/4 W
R4	270 Ohm	10%	1/4 W
R5	470 Ohm	10%	1/4 W
R6	220 KOhm	10%	1/4 W
R7	20 KOhm	10%	1/4 W
R8, R9	330 Ohm	10%	1/4 W
R10	470 Ohm	10%	1/4 W
UR1	150 Ohm	8-pin SIP	
UR2	33 KOhm	9-pin SIP	
UR3, pins 1-16	Short (0 Ohms)		
UR3, pins 2-15	8.2 KOhm	10%	1/4 W
UR3, pins 3-14	56 Ohm	10%	1/4 W
UR3, pins 4-13	15 KOhm	10%	1/4 W

CAPACITORS

Position	Value	Type	Rating
C1 to C7, C10, C11, C14 to C18, C21 to C33, C35, C36, C37	.1 uF	Bypass	
C8	33 uF	Electrolytic	>10 V
C9	200 pF		>10 V
C12, C13	>10 uF	Tantalum	>25 V
C19	.01 uF	Bypass	
C20	10 pF	Ceramic Disk	>10 V
C22	>10 uF	Tantalum	>17 V
C34	.01 uF	DIP	
UR3, pins 7-10	120 pF		>10 V

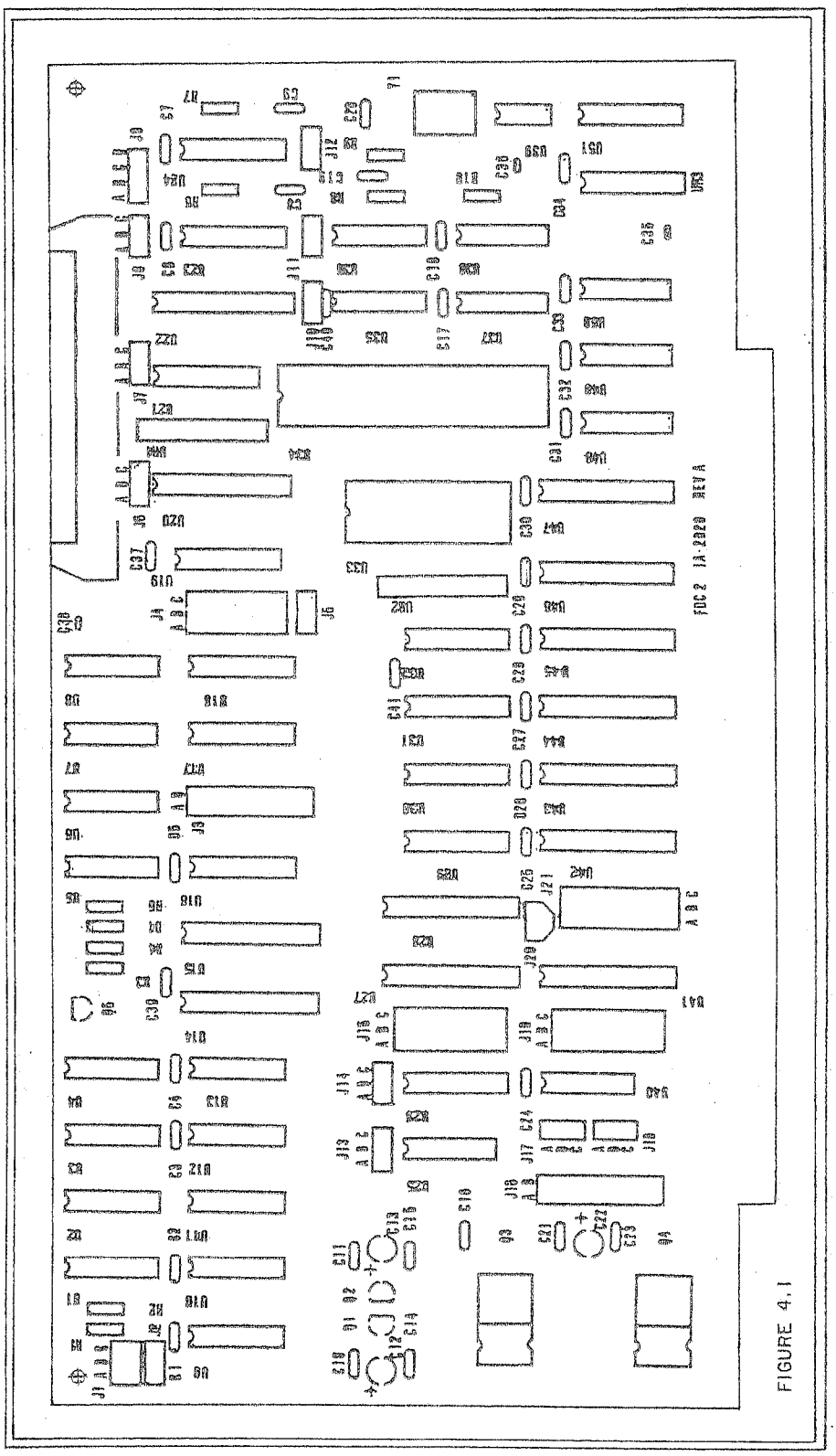


FIGURE 4.1

MISCELLANEOUS

Position	Part #	Function, Specification
Y1		16.00 MHz fundamental crystal
Q1	79L05	Low power -5 Volt regulator
Q2	78L12	Low power +12 Volt regulator
Q3, Q4	7805	+5 Volt regulator
Q5	2N2222	Transistor
D1	1N5232	5.6 Volt Zener diode

INTEGRATED CIRCUITS

Position	Part #
U1	74LS03
U2	7405
U3, U4	74LS00
U5	74LS74
U6, U7	74LS164
U8	74LS32
U9	74LS74
U10	74LS32
U11	74LS74
U12	74LS10
U13	74LS27
U14, U15	74LS240
U16	74LS157
U17	74LS151
U18	74LS155
U19	8131
U20	74S240
U21	NE590
U22	74S240
U23	74LS153
U24	96LS02
U25	74LS00
U26	74LS175
U27	25LS2521
U28	74LS373
U29, U30, U31, U32	74LS193
U33	2708
U34	uPD765
U35	74LS393
U36	74LS00
U37	74LS293
U38	74LS125
U39	CA3140
U40	7407
U41, U42	25LS2521
U43, U44	74LS244
U45, U46	8304
U47	74LS244
U48	74LS32
U49, U50	74LS74
U51	74LS124

Section 5

Revisions and Manual Applicability

5.0 Revisions and Manual Applicability

This manual references revision 0 of the FDC-2 Floppy Disk Controller Board.

Revision 0 Errors

1. DMA Error

The first ten boards of FDC-2 production contained an error in the DMA circuitry, so that the board would initiate a DMA cycle whenever the S-100 signals DMA0* and DMA1* were inactive at the same time that HOLD* and pHLDA were active, if the DMA device driving HOLD* is set to a lower DMA priority than the FDC-2. This would occur without regard to whether the FDC-2 actually needed the bus.

The error will have no effect on operation of the FDC-2 in systems where it is the only DMA device or in systems where the other DMA device or devices are set to higher priorities than the FDC-2.

The ten boards affected were all sold well before June 3, 1980.

The error is corrected by changing the board circuitry so that the board version of pHOLD* is examined rather than the S-100 bus version, by making the following cuts and jumpers:

a. On the component side of the card, cut the two traces connected to U13, pin 1. One trace goes to the left to a plated through hole; it should be cut between the plated through hole and U13, pin 1. The other trace goes to the right under the socket, and comes out between pins 13 and 14 of U13, where it may be cut.

b. JUMPER with wire wrap wire the plated through hole to the left of U13, pin 1 (mentioned above) and the plated through hole directly to the right of U14, pin 18. This reconnects the trace that was freed from U13, pin 1 in step a. (The jumper should be installed on the solder side of the card.)

c. JUMPER U13, pin 1, to U11, pin 9.

These corrections were made to all subsequent Revision 0 FDC-2 boards after the first ten, and will be incorporated in the printed circuit at Revision A.

Section 6

Ithaca Intersystems Limited Warranty

ITHACA INTERSYSTEMS LIMITED WARRANTY

All equipment manufactured by ITHACA INTERSYSTEMS shall be guaranteed against defects in materials and workmanship for a period of ninety (90) days from date of delivery to the Buyer by the Seller, and the Seller agrees to repair or replace, at its sole option, any part which proves to be defective and attributable to any defect in materials or workmanship.

> EXCEPT FOR THE WARRANTIES THAT THE GOODS ARE MADE IN A WORKMANLIKE MANNER AND IN ACCORDANCE WITH THE SPECIFICATIONS SUPPLIED, SELLER MAKES NO WARRANTY EXPRESS OR IMPLIED, AND ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE WHICH EXCEEDS THE FOREGOING WARRANTY IS HEREBY DISCLAIMED BY SELLER AND EXCLUDED FROM ANY AGREEMENT.

Buyer expressly waives its rights to any consequential damages, loss or expense arising in connection with the use of or the inability to use its goods for any purpose whatsoever.

No warranty shall be applicable to any damages arising out of any act of the Buyer, his employees, agents, patrons or other persons.

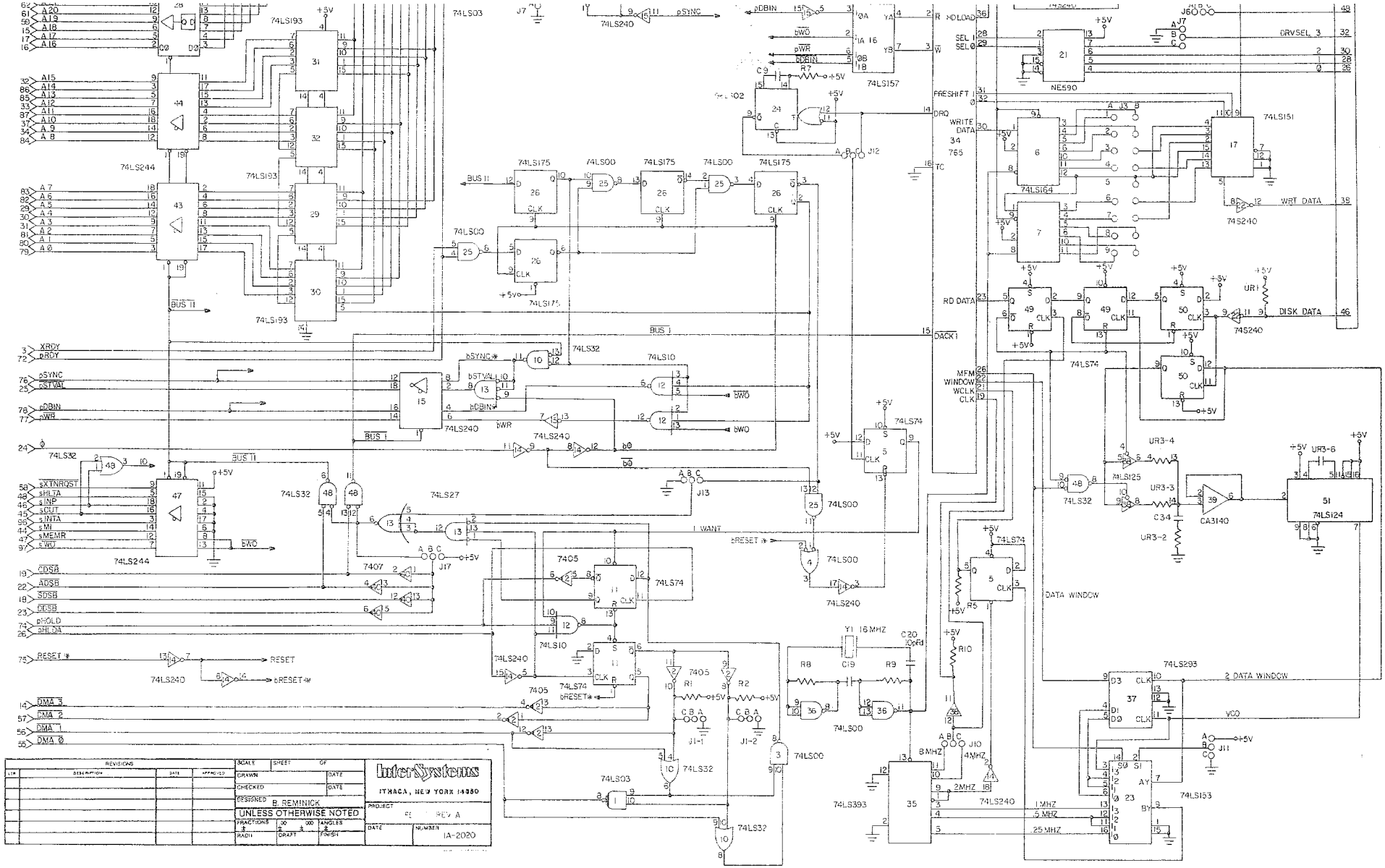
In the event that a unit proves to be defective, and after authorization by Seller, the defective part and/or unit, as authorized, must be securely packaged and returned Freight Prepaid by the Buyer to ITHACA INTERSYSTEMS for repair. Upon receipt of the unit, ITHACA INTERSYSTEMS will repair or replace, at its sole option, the defective part or product and return such part/product Freight Prepaid to the Buyer.

The remedies set forth herein are exclusive and the liability of Seller to any contract or sale or anything done in connection therewith, whether in contract, in tort, under any warranty, or otherwise, shall not, except as expressly provided herein, exceed the price of the equipment or part on which said liability is based.

This warranty is given solely to the original Buyer. No employee or representative of Seller is authorized to change this warranty in any way or grant any other guaranty or warranty.

Section 7

Schematic Diagram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74LS244
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74LS157
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74LS151
74LS164
74S240
74LS125
74LS24
74LS293
74LS153
74LS393
NE590
CA3140
7405
7407
pSYNC
pDBIN
pWR
bWO
bSTVAL
bRESET
RESET
XRDY
pRDY
SHLTA
SINP
SOUT
SINTA
SM1
SMEMR
SWO
CDSB
ADSB
SDSB
DDSB
pHOLD
SHLDA
DMA 3
DMA 2
DMA 1
DMA 0
BUS I
BUS II
R NO LOAD
SEL 1
SEL 0
DRVSEL 3
PRESHIFT
DRQ
WRITE DATA
765
TC
WRT DATA
RD DATA
DISK DATA
DACK1
MFM
WINDOW
WCLK
CLK
I WANT
DATA WINDOW
2 DATA WINDOW
VCO
Y1 16 MHZ
8 MHZ
4 MHZ
2 MHZ
1 MHZ
.5 MHZ
.25 MHZ
J1-1
J1-2
J7
J60
J11
J12
J13
J17
J10
UR1
UR3-2
UR3-3
UR3-4
UR3-6
C34
C19
C20
R5
R7
R8
R9
R10
R2
InterSystems
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B. REMINICK
UNLESS OTHERWISE NOTED
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